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FPGA Implementation of NOR Flash Storage Controller

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Abstracts

Flash storage memory devices are Nand and NOR types which are widely used in data storage application in computers and solid states drives. Flash are nonvolatile and electrically erased and reprogrammed. A flash memory controller (or flash controller) manages the data stored on flash memory and communicates with a computer or electronic device. When the system or device needs to read data from or write data to the flash storage, it will communicate with the flash controller. Flash controller is used to control programming and erasing operation of flash memory storage. FPGA builds reconfigurable environment for flash memory controller which helps in generation of exact timing specifications of flash chip. NAND Flash does not support in place updates to overcome this disadvantage of NAND storages proposed design works on NOR flash memory.

Keywords: Flash memory storage, NOR flash memory controller, FPGA, flash drives.

Introduction

Flash memory is an electronic non-volatile computer storage medium that can be electrically erased and reprogrammed. Flash memory was developed from EEPROM (electrically erasable programmable read-only memory), but it refers specifically to non-flash EEPROM which is erasable in small blocks, typically in bytes. Because erase cycles are slow, erasing flash memory in blocks gives it a significant speed advantage over non-flash EEPROM when writing large amounts of data. Flash memory stores information in an array of memory cells made from floating-gate transistors [1].

Flash memory controllers can be designed for operating in low duty cycle environments like SD cards, Compact Flashcards. Flash controllers can also be designed for higher duty-cycle environments like drives (SSD) used as data storage for laptop computer systems. Flash memory controller is used to control bit error synchronization failures and recovery of data rate. Flash memory controller is difficult to build in general purpose microcontroller system, it needs reconfigured hardware, FPGA provides platform for user configured environment. Flash memory controller is used to simplify the process of programming and erasing the memory along with taking care of all special operations required to update the flash memory contents [1].

Flash memory is used for easy and fast information storage in

1. Computers
2. Digital cameras
3. Home video game.
4. Memory Cards
5. USB Flash drives
6. Solid State drives for transfer of data between computers and other digital products.

Background study

When the system or device needs to read data from or write data to the flash storage, it will communicate with the flash controller. Devices like SD cards and USB flash drives typically have a small number of flash memory die so operations are limited to the speed of the individual flash memory die. In other hand a high-performance solid-state drive will have 100 or more die organized in a matrix and provided with parallel communication paths so that it increases speeds of operation. After manufacturing of flash storage device, the flash controller is first put to work formatting the flash memory storages, then and then only flash storages are operating properly. Because of this it maps out bad flash memory cells, and it allocates spare cells to be substituted for future failed cells. Some part of the spare cells is also used to hold the firmware which operates the controller and other special features for a particular storage device. A directory structure is created to allow the controller to convert requests for logical sectors into the physical locations on the actual flash memory chips [2, 3].

Flash storages broadly classified in to NAND and NOR types. NAND flash storages are used in USB and tablets. NOR-based flash has long erase and write times, but

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provides full address and data buses, allowing random access to any memory location. This thing makes it a suitable replacement for older read-only memory (ROM) chips. One more popular application for flash memory is as a replacement for hard disks . Flash memory does not have the latencies and mechanical limitations of hard drives, so a solid-state flash drive (SSD) is attractive when considering speed, noise, power consumption, and reliability. Flash memories are written by a host personal computer, through a permanent interface (i.e., soldered chips on circuit boards) in traditional systems. Such use of flash memory devices is common in embedded systems to store configuration information [2].

Related work

Flash memory was invented by Dr. Fujio Masuoka when he was working with Toshiba during 1980.Intel corporation launched commercial chips of NAND and NOR memories that can be replaced with ROM chips in 1988. Flash memory is a type of constantly powered nonvolatile memory that can be erased and reprogrammed in blocks [1].

Koichi S E and Hitoshi Kume in [3] have proposed simple erase and erase-verify controller with 1Mb capacity. In which all memory actions are automatically conducted in a chip without any further external control. The internal status can be checked through a status polling mode at I/O port 7 and architecture is based on a command signal latch, sequence controller, and a verify-voltage generator [3].

As flash memory capacity increases architectural designs modifies. A new design of NAND flash memory controller in FPGA was proposed by Peng Qiang and Jian Cao in [4], which was about bandwidth and different data types such as asynchronous and synchronous. They have proposed that designing of flash memory controller in FPGA environment is efficient than general purpose microcontroller systems. FSM logic helps in synchronization of command operations by flash memory [4]. Controller is designed in such a way that that user can operate flash memory without considering internal timing parameters of flash memory chip.

Lin and Dung in [5] proposed a NAND flash memory controller for SD/MMC card. They have designed a t-EC w-bit parallel BCH EEC to correct the bit flipping errors. The controller has a high reliability because of its defect management and code banking algorithm.

Flash memory controller designed in [5] gives a higher rate of data access. Such designs definitely improve the performance of a flash memory access controller. But this method cannot be adapted to every existing flash memory device. To do so the flash memory controller design has to be reconfigurable. This is why we chose a reconfigurable approach to design a custom flash memory controller; this was proposed by Omar Elkeelany and Vivekanand S. Todakar in [6]. They have proposed that a bidirectional hardware based core for the SD card design was implemented in reconfigurable FPGA based data concentrate or chip [6].

Hoeseung Jung, Sanghyuk Jung in [7] have proposed a simulator that considers all of the hardware components in SSD to assist in generating quantitatively accurate analysis when an algorithm or controller is realized. This simulator models the detailed characteristics of hardware components such as operation clock frequency and resource conflicts in order to represent SSD in great detail [7]. This overcomes the problems which were occurred during modeling of flash memory controller.

Multichannel flash memory controller which includes multiple chip parallelism which can handle many requests simultaneously. Multichannel NAND controller proposed by Soya Jose and Pradeep.C [8]. They have proposed a system where necessary control signals are generated by controller and addressed by crossbar switch, resulting in improved speed of accessing [8].

NOR flash memory controller

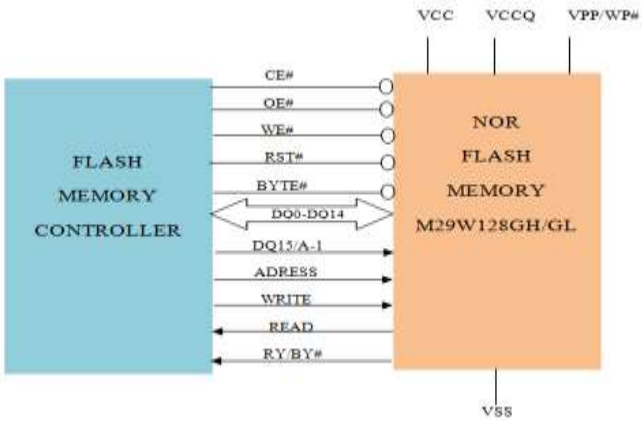

Figure 1. Logic diagram of Flash Memory Controller

For flash memory controller design NOR flash chip of micron M29W128GH/GL is used. As shown in fig.1, flash chip has many pins for operation. Flash memory chip has its own timing specification and commands. It

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is asynchronous, uniform block, parallel NOR Flash memory device manufactured on 90nm single-level cell (SLC) technology. Flash memory chip required its predefined timing specification with respect to logic diagram [9]. Table no.1 is used to convey different pin functions. It has different registers for monitoring the status of memory chip.

Serial protocol simplifies process of address data and command separation by user. It converts sequential input to differentiable bits as memory chip required.

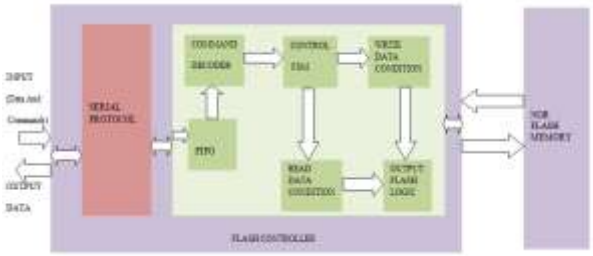

Figure 2. Block diagram of Flash Memory Controller

Table 1. Pin Out functions [9].

PIN	DESCRIPTION
A [MAX:0]	Input address bus
CE#	CHIP ENABLE active low pin used to activate chip
OE#	OUTPUT ENABLE active low pin used to control bus read operation
WE#	WRITE ENABLE active low pin controls the bus WRITE operation of the command interface.
VPP/WP#	VPP/Write Protect- it provides WRITE PROTECT function and VPPH function. These functions protect the lowest or highest block of memory.
BYTE#	Byte/word organization select - it switches between x8 and x16 bus modes. When BYTE# is LOW, the device is in x8 mode; when HIGH, the device is in x16 mode. This is active low input pin.
RST#	Active low input pin which provides hardware reset.
DQ[7:0]	Data I/O pin- Outputs the data stored at the selected address during a READ operation. During WRITE operations, they represent the commands sent to the command interface of the internal state machine.
DQ[14:8]	Data I/O pin- Outputs the data stored when BYTE# is HIGH. When BYTE# is LOW, these pins are not used and are High-Z, not used in write mode.
DQ15/A-1	Data I/O or address input pin- When the device operates in x16 bus mode, this pin behaves as data I/O, together with DQ [14:8]. When the device operates in x8 bus mode, this pin behaves as the least significant bit of the address.
RY/BY#	Ready busy pin - During PROGRAM or ERASE operations, RY/BY# is LOW, and is High-Z during read mode, auto select mode, and erase suspend mode. After hardware reset, READ and WRITE operations cannot begin until RY/BY# goes High-Z.

As shown in figure 2. According to different commands are written on command interface of the memory it perform different operations like PROGRAM or ERASE operations. Flash controller simplifies the process of programming, erasing, reading the memory by taking care of all special operations required to update the memory contents. The end of a PROGRAM or ERASE operation can be detected and any error condition can be identified. Data and input commands are first stored in FIFO. After that command decoder checks whether it received properly as per data/command sequence or any invalid data. Then it separates data and commands from input sequence. Then the operation is selected according input command i.e. whether it is READ, WRITE or PROGRAM operation. According to condition READ data condition or WRITE data condition sub codes of commands containing address and data cycles are generated [8,9]. At this all signals are generated with the timing specification which is required by flash memory. In a proposed flash memory controller it is designed to copy the collected data temporary stored in FPGA internal buffers and serial protocol is interface between a user and flash memory controller. Serial protocol is used to send and receive data and commands sequentially over a computer bus [4, 5].

Conclusion

NOR Flash devices are primarily used for reliable code storage (boot, application, OS, and execute-in-place (XIP) code in an embedded system), with some limited data storage. System design and development of reconfigurable NOR flash memory controller will help in NOR devices operate in high-speed burst or page mode for use in execute-in-place

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(XIP) environments where code runs directly from the device to minimize system boot time. NOR flash memory requires minimal ongoing management due to the underlying cell structure. This eliminates the need for external error correction code (ECC), bad block management, and wear leveling.

References

1. *NOR /NAND FLASH guide.pdf http://www.micron.com/products/nor-flash/parallel-nor-flash/download guide.pdf*
2. *L. Crippa, R. Micheloni, I. Motta and M. Sangalli," Nonvolatile Memories: NOR vs. NAND Architectures"R. Memories in Wireless Systems, C_Springer-Verlag Berlin Heidelberg 2008.*
3. *Koichi S E, Hitoshi Kume, Yuzuru Ohji"An 80-Ns 1-Mb Flash Memory With On-Chip Erase/Erase-Verify Controller" IEEE Journal Of Solid-State Circuits, Vol. 25, No. 5.October 1990.*
4. *Peng Qiang, Jian Cao, Xing Zhang, Dun-Shan Yu" A Novel NAND Flash Memory Controller Compatible with Asynchronous and Source Synchronous Data Types" 978-1-4673 2475-5/12 ©2012 IEEE.*
5. *Chuan-Sheng Lin, Lan-Rong Dung, "A NAND Flash memory controller for SD/MMC flash memory card", IEEE TRANSACTIONS ON MAGNETICS, VOL. 43, NO. 2, Feb.2007.*
6. *Omar Elkeelany and Vivekanand S. Todakar," Data Archival to SD Card Via Hardware Description Language", IEEE EMBEDDED SYSTEMS LETTERS, VOL. 3, NO. 4, DECEMBER 2011.*
7. *Hoeseung Jung, Sanghyuk Jung,"Architecture Exploration of Flash Memory Storage Controller through a Cycle Accurate Profiling". IEEE Transactions on Consumer Electronics, Vol. 57, No. 4, November 2011.*
8. *Soya Treesa Jose. Prof. Pradeep.C "Design of a Multichannel NAND Flash Memory Controller for Efficient Utilization of Bandwidth in SSDs", 978-1-4673-5090-7/13 ©2013 IEEE*
9. *Parallel NOR Flash Embedded MemoryM29W128, M29W128GL datasheet http://www.micron.com/ Parts/nor-flash/parallel-nor-flash/m29w128gh70n6e.pdf.*